

# Verification Methodology Manual For SystemVerilog By Janick Bergeron;Eduard Cerny;Alan Hunter

**By Janick Bergeron;Eduard Cerny;Alan Hunter**

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The VMM verification methodology for SystemVerilog enables engineers to build powerful and robust The VMM is defined in the Verification Methodology Manual

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In this first article in a series of tutorials based on the SystemVerilog Verification Methodology Manual, SystemVerilog reference verification methodology

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The Reference Verification Methodology The SystemVerilog implementation of the RVM is known as the VMM (Verification Methodology Manual).

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